Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of the Claims

1. (Canceled)

2. (Currently Amended) A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

a single intermediate substrate comprising a network of conductive contacts formed thereon, said intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first semiconductor die and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through, and

one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage;

a printed circuit board positioned such that a first surface of said printed circuit board faces said intermediate substrate;

a plurality of topographic contacts extending from said intermediate substrate to said first surface of said printed circuit board;

at least one decoupling capacitor mounted to ~~said first surface of~~ said intermediate substrate and conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension (a) of said decoupling capacitor is ~~accommodated in a space defined by~~ less than or equal to a thickness dimension (b) of a topographic contact conductively coupled to a conductive contact on ~~said first surface of~~ said intermediate substrate; and

a heat sink including a cap portion and a peripheral portion, wherein

said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor die, and

said peripheral portion engages ~~a mounting zone defined by a lateral dimension of~~ said intermediate substrate.

3.-7. (Canceled)

8. (Currently Amended) A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate comprising a network of conductive contacts formed thereon, said intermediate substrate positioned between said first active surface of said first semiconductor die and said second active surface of said second semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second active surface, wherein

said first semiconductor die is electrically coupled to said intermediate substrate by at least one topographic contact extending from said first active surface to said first surface of said intermediate substrate,

said intermediate substrate defines a passage there through,

said second semiconductor die is secured to said second surface of said intermediate substrate such that said conductive bond pad of said second semiconductor die is aligned with said passage, and

said second semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said first surface of said intermediate substrate;

at least one decoupling capacitor mounted to ~~said first surface of~~ said intermediate substrate and conductively coupled between high and low voltage inputs of said first or second semiconductor dies, wherein a thickness dimension (a) of said decoupling capacitor is ~~accommodated in a space defined by~~ less than or equal to a thickness dimension (b) of a topographic contact conductively coupled to a conductive contact on ~~said first surface of~~ said intermediate substrate; and

a heat sink including a cap portion and a peripheral portion, wherein

said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor dies, and

said peripheral portion ~~engages a mounting zone defined by a lateral dimension of~~ is mounted to said intermediate substrate extending beyond a periphery of at least one of said first and second semiconductor dies.

9.-15. (Canceled)

16. (Original) A printed circuit board assembly as claimed in claim 2, wherein said printed circuit board assembly is resident in a computer system comprising a programmable controller and at least one memory unit, wherein said memory unit comprises said printed circuit board assembly.

17.-22. (Canceled)

23. (Currently Amended) A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

a single intermediate substrate comprising a network of conductive contacts formed thereon, said intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first

semiconductor die and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through, and

one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage, and wherein said first semiconductor die and said second semiconductor die span across said passage;

a printed circuit board positioned such that a first surface of said printed circuit board faces said intermediate substrate;

a plurality of topographic contacts extending from said intermediate substrate to said first surface of said printed circuit board; ~~and~~

at least one decoupling capacitor mounted to said intermediate substrate and conductively coupled to one of said first or second semiconductor dies, wherein a thickness dimension (a) of said decoupling capacitor is less than or equal to either a thickness dimension (b) of a topographic contact conductively coupled to a conductive contact on said intermediate substrate or a thickness dimension (c) of said first semiconductor die; and

a heat sink including a cap portion and a peripheral portion, wherein

said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor dies, and

said peripheral portion ~~engages a mounting zone defined by a lateral dimension of~~is mounted to said intermediate substrate~~ extending beyond a periphery of at least one of said first and second semiconductor dies~~.